Low Voltage and Low Power CMOS Exponential-Control Variable-Gain Amplifier

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SUMMARY A compact, low voltage, low power and wide output operating range CMOS exponential-control variable-gain amplifier has been presented. The gain control range of the proposed variable-gain amplifier can be about 50.7 dB while the maximum linearity error is about -1.09%. For the case of supply voltage $V_{DD} = 2$ V, the maximum power dissipation is only 1.6 $\mu$W. The proposed circuit has been fabricated in a 0.5 $\mu$m 2p2m N-well CMOS process. Experimental results are given to confirm the feasibility of the proposed variable gain amplifier. The proposed circuit is expected to be useful in analog signal processing applications.

key words: CMOS, low voltage, low power, exponential-control, VGA

1. Introduction

Variable-gain amplifiers (VGA) can be widely used in analog signal processing such as disk drives [1], telecommunications [2], [3] and automatic gain control (AGC) circuits [4], [5]. Traditionally, a VGA can be realized by a multiplier with an input signal and an exponential one [5], [6]. Recently, a VGA without multiplier has been reported [8], [9], however, since the exponential signal is generated by a pseudo-exponential function, i.e., $f(x) = \left(\frac{x}{nUT}\right)^{\frac{1}{n}} \approx e^x$, where $|x| < 1$ [7]–[9], therefore the exponential-control range can only be about 15 dB. In this Letter, a compact, low voltage and low power CMOS exponential-control VGA is developed. There is no multiplier used in the design and the exponential signal is given by using the $V-I$ characteristics of the MOSFET in weak-inversion region. The gain range of the proposed VGA can be 50.7 dB and also the gain can be adjusted by two controlled voltages. The proposed circuit has been fabricated in a 0.5 $\mu$m 2p2m N-well CMOS process and the experimental results are given to demonstrate the proposed VGA.

2. Circuit Implementation

The proposed VGA is shown in Fig. 1. Assume that M1-M4 are biased in the weak inversion region, their $V-I$ characteristics [10] can be given as

$$I_1 = I_{in} + I_B = I_{D03} \cdot \exp \left(\frac{(V_{DD} - V_1) + (n-1)V_{SB1}}{nU_T}\right)$$

(1)

From Eqs. (3) and (4), one can have

$$I_4 = I_B \cdot \exp \left(\frac{(V_1 - V_2)}{nU_T}\right)$$

(6)

Assume that M5 and M6 are operated in saturation and it will have

$$I_5 = I_6 = I_4$$

(7)

From Eqs. (5)–(7), the output current $I_{out}$ can be given as

$$I_{out} = I_2 - I_5 = I_{in} \cdot \exp \left(\frac{(V_1 - V_2)}{nU_T}\right)$$

therefore

$$\frac{I_{out}}{I_{in}} = \exp \left(\frac{(V_1 - V_2)}{nU_T}\right)$$

(8)
According to Eq. (8), a variable-gain amplifier can be realized and its gain can be exponentially controlled by the controlled voltages \( V_1 \) and \( V_2 \). Since M1-M4 are biased in the weak inversion region, the power dissipation can be very low. Besides, there is only two transistors cascoded in the supply voltage path, it can operate under low supply voltage.

3. Experimental Results

The proposed VGA has been fabricated in a 0.5 \( \mu \text{m} \) 2p2m N-well CMOS process and the PMOSFETs are embedded in individual wells. The die photograph is shown in Fig. 2. The aspect ratios of the transistors of the proposed VGA are all \( \left( \frac{W}{L} \right) = \left( \frac{1 \mu \text{m}}{1 \mu \text{m}} \right) \). For a MOSFET to operate in the weak inversion region, the drain current must comply with the following requirement [11]:

\[
I_D < 2n \frac{K_p W}{L} U_T^2
\]  

(9)

The threshold voltage for the NMOS transistor is 0.78 V and that for the PMOS transistor is −1.1 V in our process and the supply voltage in the experiment is 2 V. According to Eq. (9), the bias current \( I_B \) was set to 0.08 \( \mu \text{A} \). The measured maximum power consumption is 1.6 \( \mu \text{W} \). The experimental results are shown in Fig. 3 where the input current \( I_{in} \) was 0.07 \( \mu \text{A} \). As the controlled voltage \( V_1 \) varies from 0.55 V to 0.8 V (while \( V_2 = 0.7 \text{ V} \)), the measured gain range can be 50.7 dB. However, as the input current was increased to 0.12 \( \mu \text{A} \), the measured gain range can be about 45 dB. As the supply voltage is reduced to 1.9 V and 1.8 V, respectively; under the same test conditions, the corresponding gain ranges are about 46.3 dB (from −24.56 dB to 21.75 dB) and 40.1 dB (from −21.16 dB to 18.92 dB), respectively. Figure 4 shows the error between the measured result and the theoretical values calculated by Eq. (8). The maximum measured error was −1.09%. The experimental results verify the theoretical analysis calculated by Eq. (8).

The frequency response of the proposed VGA is shown in Fig. 5 which were performed with the controlled voltages \( V_1 = 0.68 \text{ V} \) and 0.73 V, respectively, and the controlled voltages \( V_2 = 0.7 \text{ V} \). The corresponding −3 dB bandwidth can be 228 kHz and 134 kHz, respectively. The summary of the experimental results is listed in Table 1.

4. Conclusions

In this Letter, a low voltage and low power CMOS VGA has been developed. Experimental results have been given
to confirm the validity of the theoretical analysis. The proposed circuit is expected to be useful in the design of an AGC and other analog signal processing applications.

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References