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PAPER Special Section on Analog Circuit Techniques and Related Topics

Low-Voltage CMOS Voltage-Mode Divider and Its Application

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SUMMARY A CMOS voltage-mode divider, which can operate for low supply voltage and low power dissipation, is presented in this paper. The proposed voltage-mode divider can be used to realize a pseudo-exponential function generator. The experimental results of the proposed voltage-mode divider show that, under the supply voltage V_{DD}=2.5 V, the linearity error is less than 1.18% and the power consumption is only 102 μW. Also the proposed pseudo-exponential function generator exhibits a 15 dB output dynamic range and the linear error is less than1.54%. Both the proposed circuits have been fabricated in a 0.5 μm N-well CMOS 2P2M process. The proposed circuits are expected to be useful in analog signal processing applications.

key words: *low-voltage, CMOS, divider*

1. Introduction

In the past decade, the demand for portable operation of electronic systems has lead to the trend of designing circuits to operate for low supply voltages [1]–[7]. In another hand, the higher packing densities offered by the modern VLSI technology also increases the power dissipation per chip area. In order to reduce the power dissipation, the scaling down supply voltage can be used. Although scaling down supply voltage might not consequently lower down the power dissipation for analog circuits, however, it is generally true for mixed-mode systems where most of them are digital circuits. The analog divider is an important building block in the design of signal conditioning and processing circuits, such as analog computation, fuzzy control, neural network, A/D converters and instrumentation circuits [8]–[12], etc. However, among those reported works, none of them is designed to operate for low supply voltage; therefore, the development of the low-voltage analog dividers is necessary. In this paper, a new low-voltage CMOS voltage-mode divider is presented; the proposed circuit can operate for a single supply voltage of 2.5 V. The application of the proposed low-voltage voltage-mode divider is also given. The proposed circuits have been fabricated in a 0.5 μm N-well CMOS 2P2M process and the experimental results are given to demonstrate the proposed circuits.

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2. Circuit Description

The proposed low-voltage voltage-mode divider is shown in Fig. 1. Assume that both M1 and M2 are biased in saturation without the body effect. According to the square-law characteristics of MOSFETs, the drain currents of M1 and M2 can be written as

$$I_1 = \frac{K_{n1}}{2}(V_1 - V_{Tn1})^2 \tag{1}$$

and

$$I_2 = \frac{K_{n2}}{2}(V_2 - V_{Tn2})^2 \tag{2}$$

where $K_{n1,2}$ are the transconductance parameters and $V_{Tn1,2}$ are the threshold voltages of M1 and M2, respectively. The current mirror, composed of M5 and M6, is used to generate the current I_5 and I_6, therefore I_6=I_5=I_1. If M1 and M2 are perfectly matched, i.e., K_{n1}=K_{n2}=K_n and V_{Tn1}=V_{Tn2}=V_{Tn}, one can have

$$I_{11} = I_1 - I_2 = \frac{K_n}{2}[(V_1 - V_{Tn})^2 - (V_2 - V_{Tn})^2] \tag{3}$$

Assume that both M3 and M4 are biased in triode region without the body effect. One can have

$$I_4 = \frac{K_{n4}}{2}\left(2(V_4 - V_{Tn4})V_{DS4} - V_{DS4}^2\right) \tag{4}$$

and

$$I_7 + I_{11} = \frac{K_{n3}}{2}\left(2(V_3 - V_{Tn3})V_{DS3} - V_{DS3}^2\right) \tag{5}$$

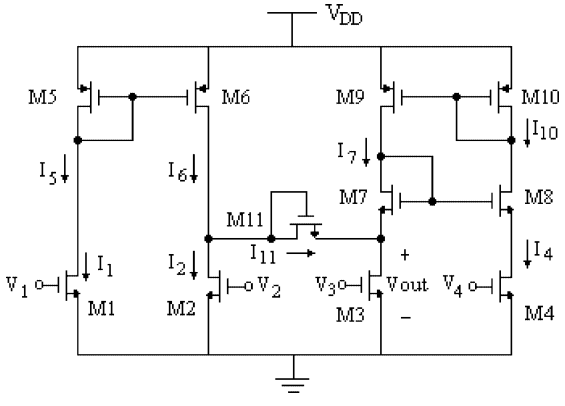


Fig. 1 Proposed low-voltage voltage-mode divider.

The transistor M11 in Fig. 1 is used to generate a voltage drop from the drain of M2 to the drain of M3, which will ensure that M2 is biased in saturation and M3 is biased in triode region. The current mirror, composed of M9 and M10, is used to generate the currents I_7 and I_{10}, so that

$$I_7 = I_{10} = I_4 \tag{6}$$

Assume that M7 and M8 are perfectly matched (i.e., $K_{n7} = K_{n8}$ and V_{Tn7}=V_{Tn8}) and both of them are biased in saturation. According to the square-law characteristics of MOSFETs, the following equation can be obtained.

$$V_{GS7} = V_{GS8} = \sqrt{\frac{2I_4}{K_{n7}}} + V_{Tn7} \tag{7}$$

Since $V_{GS8} + V_{DS4} = V_{GS7} + V_{DS3}$ and according to Eq. (7), one can have

$$V_{DS3} = V_{DS4} \tag{8}$$

Because that the source voltages of M7 and M8 are equal, i.e., V_{SB7}=V_{SB8}, the assumption that V_{Tn3}=V_{Tn4} is reasonable. Substituting Eqs. (4), (6) and (8) into Eq. (5) and assuming that M3 and M4 are perfectly matched (i.e., K_{n3}=K_{n4}=K_n and V_{Tn3}=V_{Tn4}=V_{Tn}), one can have

$$V_{DS3} = \frac{I_{11}}{K_n(V_3 - V_4)} \tag{9}$$

Let V_1=V_{b1}+V_N and V_2=$V_{b1} - V_N$, where V_{b1} is a DC bias voltage. According to Eq. (3), one can have

$$I_{11} = 2K_n \cdot V_N \cdot (V_{b1} - V_{Tn}) \tag{10}$$

Let V_3=$V_{b2} + V_D$ and V_4=$V_{b2} - V_D$, where V_{b2} is also a DC bias voltage. According to Eq. (9), one can have

$$V_{DS3} = \frac{I_{11}}{2K_n \cdot V_D} \tag{11}$$

Substituting Eq. (10) into Eq. (11), one can have

$$V_{out} = V_{DS3} = (V_{b1} - V_{Tn}) \cdot \frac{V_N}{V_D} \tag{12}$$

From Eq. (12), a voltage-mode divider can be realized.

Although there are three transistors cascoded between the supply voltage and ground, however, since M3 and M4 are biased in triode region, the drain voltages of M3 and M4 must be lower than their gate voltages by the magnitude of, at least, one threshold voltage, therefore, the proposed voltage-mode divider can work for low supply voltage. To keep the proposed low-voltage voltage-mode divider work properly, M1 and M2 should be biased in saturation, therefore, the limitations of the input voltage V_N can be given as

$$V_{b1} \pm V_N > V_{Tn} \tag{13}$$

and

$$V_{b1} - V_{out} - \sqrt{\frac{2I_{11}}{K_{n11}}} - V_{Tn} - V_{Tn11} \le V_N \tag{14}$$

where V_{Tn} is the threshold voltage of M1 and M2, V_{Tn11} and K_{n11} are the threshold voltage and transconductance parameter of M11, respectively. Moreover, since the current I_{11} must flow into the drain of M3, the gate voltage of M3 should be larger than that of M4. Consequently, one can have

$$V_{b2} + V_D > V_{b2} - V_D > V_{Tn} \tag{15}$$

where V_{Tn} is the threshold voltage of M3 and M4. Next, for M3 to operate in triode region, the output range can be derived as

$$V_{out} \le V_{b2} + V_D - V_{Tn} \tag{16}$$

3. Transistor Mismatched Analysis

3.1 Mismatch between M1 and M2

If the threshold voltages of M1 and M2 are mismatched, for example, $V_{Tn1} = V_{Tn}$ and $V_{Tn2} = V_{Tn} + \Delta V_{Tn}$, respectively, Eq. (12) can be written as

$$V_{out} = (V_{b1} - V_{Tn}) \cdot \frac{V_N}{V_D} + \frac{2(V_{b1} - V_{Tn}) \cdot \Delta V_{Tn} - \Delta V_{Tn}^2}{4V_D} \tag{17}$$

According to Eq. (17), the threshold voltage mismatch between M1 and M2 will cause the nonlinear error of the proposed voltage-mode divider and the error is reversely proportional to the input voltage V_D. Because both the sources and substrates of M1 and M2 are connected to ground, the variation of threshold voltages of M1 and M2 due to the body effect could be minimized. However, in order to reduce the nonlinear errors in Eq. (17), careful layout considerations are necessary.

If the transconductance parameters of M1 and M2 are mismatched, for example, $K_{n1} = K_n$ and $K_{n2} = K_n + \Delta K_n$, respectively, Eq. (12) can be written as

$$V_{out} = V_{DS3} = (V_{b1} - V_{Tn}) \cdot \frac{V_N}{V_D} - \frac{\Delta K_n \cdot V_N(V_{b1} - V_{Tn})}{K_n V_D} \tag{18}$$

According to Eq. (18), the variation of the transconductance parameters of M1 and M2 will contribute the non-linearities of the proposed voltage-mode divider. However, if the nonlinearities are serious, the long channel devices can be used to reduced the deviation.

3.2 Mismatch between M3 and M4

If the threshold voltages of M3 and M4 are mismatched, for example, $V_{Tn3} = V_{Tn}$ and $V_{Tn4} = V_{Tn} + \Delta V_{Tn}$, respectively, Eq. (12) can be written as

$$V_{out} = V_{DS3} = (V_{b1} - V_{Tn}) \cdot \frac{V_N}{V_D + \Delta V_{Tn}} \tag{19}$$

From Eq. (19), a nonlinear error is caused by the mismatch between the threshold voltages of M3 and M4. Since both the sources and substrates of M3 and M4 are connected to ground, M3 and M4 are immune to the body effect. However, careful layout considerations are still important.

If the transconductance parameters of M3 and M4 are mismatched, for example, $K_{n3} = K_n$ and $K_{n4} = K_n + \Delta K_n$, respectively, Eq. (12) can be written as

$$V_{out} = (V_{b1} - V_{Tn}) \cdot \frac{V_N}{V_D} + \frac{\Delta I}{K_n V_D} \tag{20}$$

where

$$\Delta I = \frac{\Delta K_n}{2}\left(2(V_{b2} - V_{in} - V_{Tn})V_{out} - V_{out}^2\right) \tag{21}$$

From Eqs. (20) and (21), a nonlinear error is caused by the variation of the transconductance parameters of M3 and M4. If the non-linearities are serious, the long channel devices can be used to reduced the error.

4. Application—A Pseudo-Exponential Function Generator

A pseudo exponential function can be written as [13], [14]

$$\exp(2x) \cong \left(\frac{1+x}{1-x}\right) \tag{22}$$

The proposed pseudo exponential function generator using the proposed divider is shown in Fig. 2. Assume that, the transconductance parameters and threshold voltages of M1a–M2a are identical to those of M1–M4 in Fig. 1, one can have

$$\begin{aligned} I_{11} &= (I_1 - I_2) + (I_{1a} - I_{2a}) \\ &= \frac{K_n}{2}[(V_1 - V_{Tn})^2 - (V_2 - V_{Tn})^2 + (V_{1a} - V_{Tn})^2 \\ &\quad - (V_{2a} - V_{Tn})^2] \end{aligned} \tag{23}$$

Substituting Eq. (22) into Eq. (9) and let $V_{1a} = V_b + V_c$, $V_{2a} = V_b - V_c$, $V_1 = V_3 = V_b + V_{in}$, and $V_2 = V_4 = V_b - V_{in}$; where V_b is a bias voltage, V_c is a controlled voltage and V_{in} is the input voltage, respectively; one can have

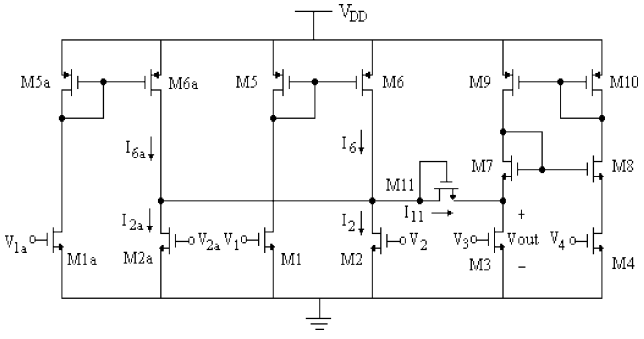


Fig. 2 Proposed pseudo-exponential function generator.

$$V_{out} = (V_b - V_{Tn})\left(\frac{1 + \frac{V_{in}}{Vc}}{1 - \frac{V_{in}}{Vc}}\right) \tag{24}$$

Comparing Eq. (24) with Eq. (22), one can have

$$V_{out} \approx b \cdot \exp(aV_{in}); \quad \text{if} \quad |aV_{in}| \ll 1 \tag{25}$$

where $a = \frac{2}{Vc}$ and $b = (V_b - V_{Tn})$. According to Eq. (25), a pseudo-exponential function generator can be realized.

5. Experimental Results

The proposed low-voltage voltage-mode divider has been fabricated in a 0.5 μm N-well CMOS 2P2M process. The die photograph is shown in Fig. 3. The aspect ratios of the NMOS and PMOS transistors for the proposed circuit are listed in Table 1. The threshold voltage for the NMOS transistor is 0.78 V and that for the PMOS transistor is −1.08 V in our process and the supply voltage in the experiment is V_{DD}=2.5 V.

The experimental results of the proposed low-voltage voltage-mode divider are shown in Figs. 4(a) and 4(b). The experiments were performed with the bias voltages V_{b1}=1.05 V, V_{b2}=1.25 V and V_D=0.5 V, 0.6 V, 0.7 V, 0.8 V and 0.9 V, respectively, while V_N varies from 0–0.5 V. The measured output offset voltage is less than 1.1 mV under all situations. Figure 5 shows the errors between the measured results and the theoretical values calculated by Eq. (12). The maximum measured error was 1.18% which

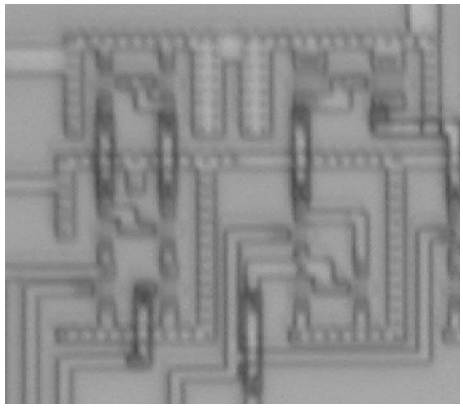
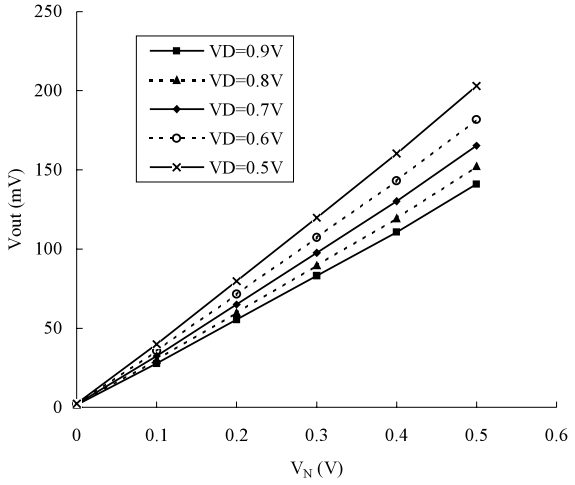


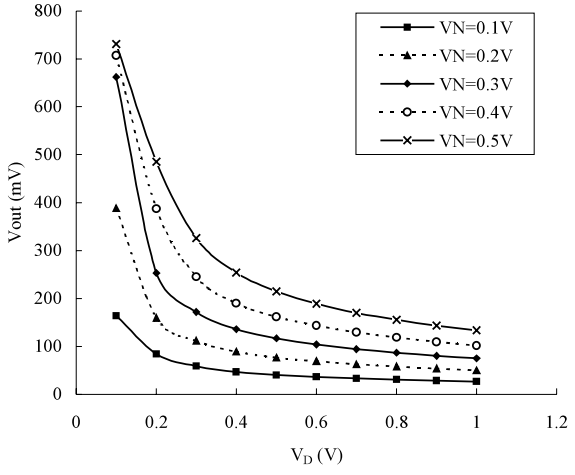
Fig. 3 The die photo of the proposed low-voltage voltage-mode divider.

Table 1 The aspect ratios of the proposed low-voltage voltage-mode divider in Fig. 1.

Transistors	Aspect ratio (μm/μm)
M1−M4, M9−M11	(2/2)
M5, M6	(6/2)
M7, M8	(2.5/2)



(a) V_{out} vs. V_N.



(b) V_{out} vs. V_D.

Fig. 4 Experimental results of the proposed low-voltage voltage-mode divider.

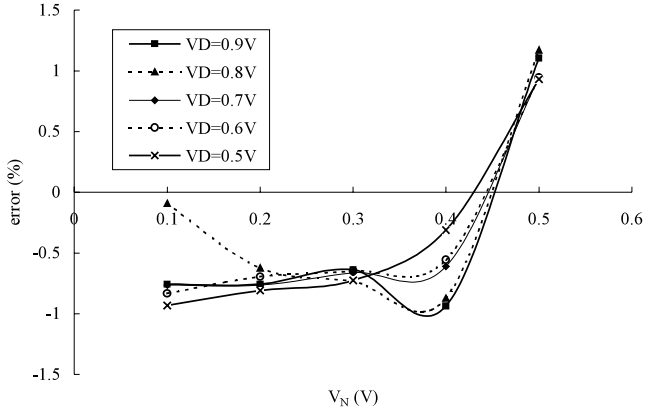


Fig. 5 Errors between the measured results and the theoretical values of the proposed low-voltage voltage-mode divider.

occurred at V_D=0.8 V and V_N=0.5 V; however, most of the measured errors are within ±1%. The measured maximum power consumption is 102 μW which occurred at V_D=0.9 V and V_N=0.5 V. The experimental results verify the theoretical analysis calculated by Eq. (12). The frequency response of the proposed low-voltage voltage-mode divider is shown in Fig. 6, which was performed with the DC voltage V_D=0.7 V, V_N=0.5 V and the magnitude of the small signal was 0.05 V. The measured corresponding −3 dB bandwidth can be 12.8 MHz.

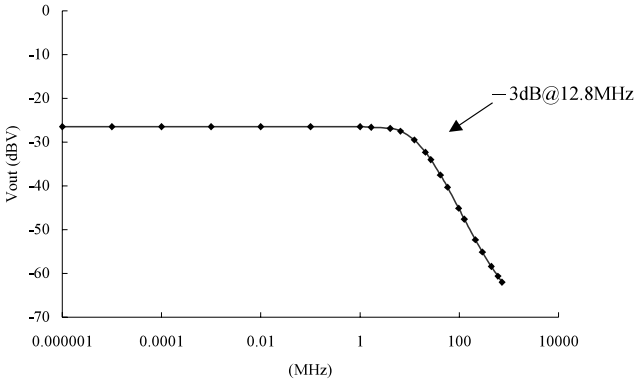
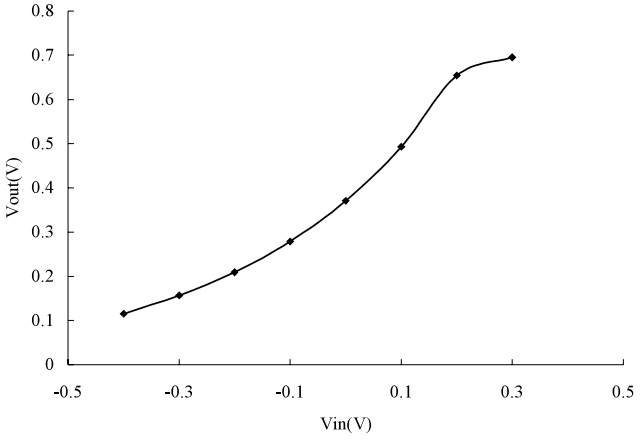
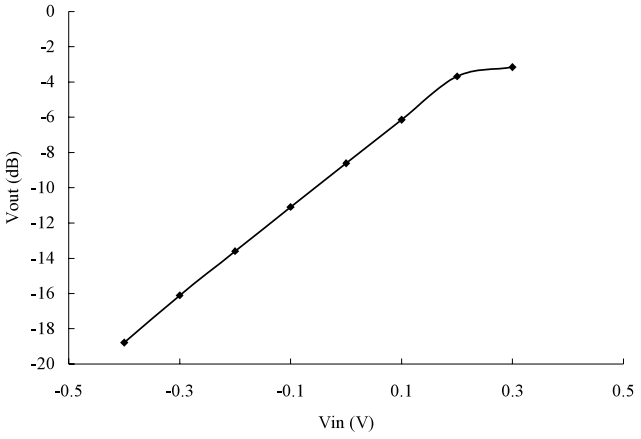


Fig. 6 Frequency response of the proposed low-voltage voltage-mode divider.



(a) Linear scale.



(b) Semi-logarithmic scale.

Fig. 7 Experimental results of the proposed the proposed pseudo-exponential function generator.

The experimental results of the proposed pseudo-

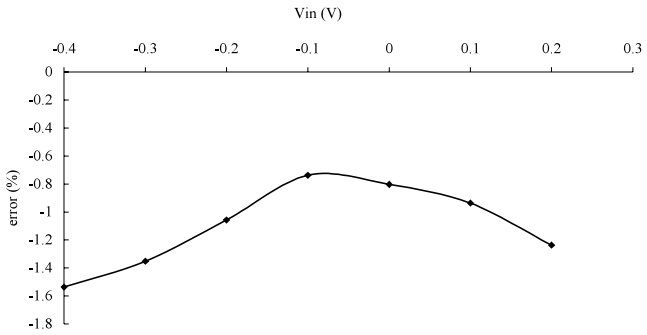


Fig. 8 Errors between the measured results and the theoretical values of the proposed pseudo-exponential function generator.

exponential function are shown in Figs. 7(a) and 7(b). The experiment was performed with the bias voltage V_b=0.95 V and the controlled voltage V_c=0.5 V. As the input voltage V_{in} varies from −0.4 V to 0.2 V, the output voltage shows an operating range of 15 dB. Figure 8 shows the errors between the measured results and the theoretical values calculated by Eq. (25). The maximum measured error is −1.54%, which occurred at $V_{in} = -0.4$ V. The experimental results confirm the theoretical analysis calculated by Eq. (25).

6. Conclusions

In this paper, a new low-voltage CMOS voltage-mode divider operating for 2.5 V supply voltage is developed. The effects of the mismatch among transistors are also discussed. Experimental results have been given to confirm the validity of the theoretical analysis. As an application, the proposed voltage-mode divider is used to realize a pseudo-exponential function generator. The proposed low-voltage voltage-mode divider and the pseudo-exponential function generator are expected to be useful in other analog signal processing applications.

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