A Low-power and Low-voltage Cube-law Circuit Design using MOSFETs

Weihsing Liu*, Wei-Lung Mao, Jyh Sheen

Abstract—A new MOSFET-based cube-law circuit is presented in this paper. The proposed cube-law circuit is featured with low power-consumption and it is also suitable for low supply-voltage operation. According to the HSPICE simulation results, under the supply voltage of 1.5 V, the input range of the proposed cube-law circuit can be 200 mV, and the corresponding maximum power dissipation is only 10.72 μW. The proposed circuit is expected to be useful in signal processing applications.

Key words: MOSFET, weak inversion, exponential.

I. INTRODUCTION

Traditionally, the cube-law circuit (cuber) is an important building block for function generation and analogue computation in communication and instrumentation systems [1-4]. However, unlike the squaring circuits [5-9], the cube-low circuits are very rare to see in recent years [10]. In the past decade, the demand for portable operation of electronic systems has lead to the trend of designing circuits to be featured with low power-dissipation and low supply-voltage operation. One possible method to realize the low-power dissipation circuit is to operate MOSFETs in the weak inversion region. Based on the exponential characteristics of the MOSFETs in weak inversion region, many analogue computational circuits have been successfully implemented [11-14]. In this paper, a new CMOS low-power and low-voltage cube-law circuit, which biasing MOSFETs in weak inversion region, has been presented. The proposed circuit was simulated with the HSPICE by using a 0.35 μm 2p4m N-well CMOS process. The simulation results are given to demonstrate the proposed circuit.

II. CIRCUIT IMPLEMENTATION

A. Design Principle

According to the Taylor’s series expansion, a general exponential function can be expressed as

\[ \exp(x) = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \ldots + \frac{x^n}{n!} + \ldots \]

(1)

Supposed that \( x \ll 1 \), the higher order terms of the Taylor’s series expansion can be neglected and eqn.(1) can be approximated as

\[ \exp(x) \approx 1 + x + \frac{x^2}{2} \]

(2)

The error between \( 1 + x + \frac{x^2}{2} \) and \( \exp(x) \) is plotted in Fig. 1, from which we can see that, if \( |x| \leq 0.2 \), the corresponding error might be less than \( 0.16\% \).

\[ \text{error} = \left| \frac{\exp(x) - \left(1 + x + \frac{x^2}{2}\right)}{\exp(x)} \right| \times 100\% \]

![Fig. 1 Errors between "exp(x)" and the function "1+x+x^2/2"

Consider the exponential function generating cell shown in Fig.2 [15, 16] where \( I_b \) is a bias current. Assume that both M1 and M2 are perfectly matched and both biased in the weak inversion region. The V-I characteristics of the MOSFET in weak inversion can be given as [17]

\[ I_b = I_{b0} \cdot \exp \left( \frac{(V_{dd} - V_b) + (n-1)(V_{dd} - V_b)}{nU_T} \right) \]

(3)

and

\[ I_o = I_{o0} \cdot \exp \left( \frac{(V_{dd} - V_b) + (n-1)(V_{dd} - V_b)}{nU_T} \right) \]

(4)

where \( n \) is the slope factor, \( U_T = kT/q \) is the thermo-dynamic voltage, \( I_{b0} \) is the leakage current, and \( V_b \) is the body
From eqns. (11) and (12), one can have
\[ I_O = I_b \cdot \exp \left( \frac{V_C - V_{b6}}{nU_T} \right) \]  
(5)

respectively. If the voltages \( V_{A1} - V_{A6} \) and \( V_{B1} - V_{B6} \) in Fig.3 are given as shown in Table I, where \( V_C \) is a bias voltage, then from eqns. (7 - 12) the currents \( I_{o1} \) and \( I_{o2} \) can be given as

\[ I_{o1} = I_{o6} = 2I_b \cdot \exp \left( \frac{(V_{A1} - V_{b6})}{nU_T} \right) \]  
(12)

**TABLE I**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>( V_{A1} )</th>
<th>( V_{A4} )</th>
<th>( V_{A6} )</th>
<th>( V_{B4} )</th>
<th>( V_{B5} )</th>
<th>( V_{A2} )</th>
<th>( V_{A3} )</th>
<th>( V_{A5} )</th>
<th>( V_{B3} )</th>
<th>( V_{B6} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>( V_C + V_{in} )</td>
<td>( V_C + V_{in} )</td>
<td>( V_C )</td>
<td>( V_C )</td>
<td>( V_C )</td>
<td>( V_C )</td>
<td>( V_C )</td>
<td>( V_C )</td>
<td>( V_C )</td>
<td>( V_C )</td>
</tr>
</tbody>
</table>

**B. Proposed Circuit**

The proposed cube-law circuit is shown in Fig.3, where six identical exponential function generating circuits, which shown in Fig.2, are used.

Assume that all the transistors of the exponential function generating circuits in Fig. 3 are biased in the weak inversion region. According to eqn. (6), the current \( I_{o1} \) - \( I_{o6} \) can be given as

\[ I_{o1} = I_b \cdot \exp \left( \frac{V_{A1} - V_{b1}}{nU_T} \right) \]  
(7)
\[ I_{o2} = I_b \cdot \exp \left( \frac{V_{A2} - V_{b2}}{nU_T} \right) \]  
(8)
\[ I_{o3} = 2I_b \cdot \exp \left( \frac{V_{A3} - V_{b3}}{nU_T} \right) \]  
(9)
\[ I_{o4} = I_b \cdot \exp \left( \frac{V_{A4} - V_{b4}}{nU_T} \right) \]  
(10)
\[ I_{o5} = I_b \cdot \exp \left( \frac{V_{A5} - V_{b5}}{nU_T} \right) \]  
(11)

\[ I_{o6} = 2I_b \cdot \exp \left( \frac{(V_{A6} - V_{b6})}{nU_T} \right) \]  
(12)

and

\[ I_{o6} = 2I_b \cdot \exp \left( \frac{(V_{A6} - V_{b6})}{nU_T} \right) \]  
(12)

By using the identity that \( \exp(a+b) = \exp(a) \cdot \exp(b) \), and according to eqn. (2), equns. (13) and (14) can be rewritten as

\[ I_{o1} = I_{o6} = I_b \cdot \exp \left( \frac{V_{A1} - V_{b6}}{nU_T} \right) \]  
(13)
\[ I_{o2} = I_b \cdot \exp \left( \frac{V_{A2} - V_{b6}}{nU_T} \right) \]  
(14)

respectively. From Fig.3, the output voltage \( V_{out} \) can be given as

\[ V_{out} = I_{o1}R_1 - I_{o2}R_2 \]  
(17)

If \( R_1 = R_2 = R \), substituting eqns. (15) and (16) for currents \( I_{o1} \) and \( I_{o2} \), and also replacing the term \( \exp(zV_o/nU_T) \) in eqns. (15) and (16) with \( [V_o/nU_T]^2/2z(V_o/nU_T)+1 \), then \( V_{out} \) can be obtained as

\[ V_{out} = I_b \cdot \frac{2V_{in}^2}{(nU_T)^2} - R \]  
(18)

From eqn. (18), a cube-law circuit can be realized. Since the transistors in the proposed cube – law circuit are
operated in the weak inversion region, the overall power consumption of the proposed circuit is very low. Moreover, the bias currents in Fig. 3 can be realized by using a single transistor, therefore there are only two transistors stacked between the power – rail and ground, hence the proposed cube – law circuit is suitable for low supply – voltage operation.

C. Mismatch analysis

If the bias currents of the proposed cube – law circuit are not identical due to process variation, for example, the bias current of exponential function generating cell Exp1 and Exp5 are \( I_b + \Delta I_{b5} \) and \( I_b + \Delta I_{b0} \), respectively. According to eqns. (7 – 17), eqn. (18) can be rewritten as

\[
V_{av} \approx I_b \cdot \frac{2V_v}{(nU_T)^2} \cdot R + \left[ \frac{\Delta I_{b5}}{I_{b5}} \cdot \exp \left( \frac{2V_v}{nU_T} \right) - \frac{\Delta I_{b0}}{I_{b0}} \cdot \exp \left( -\frac{2V_v}{nU_T} \right) \right] \cdot R
\]

From eqn. (19), a non – linear deviation is generated. If the deviation in eqn. (19) is serious, an accurate current generation circuit should be used to improve it.

Besides the bias-current mismatch, the leakage current \( I_{b0} \) of the MOSFET in weak inversion region is proportional to the aspect ratio of the MOSFET [11], therefore, the aspect ratios of M1 and M2 in Fig. 2 might also be mismatched due to process variation, which would result in the leakage current of M1 and M2 not identical. Assume that the leakage currents of M1 and M2 in Fig. 2 are \( I_{b0} \) and \( I_{b0} + \Delta I_{b0} \), respectively. According to eqns. (3) and (4), eqn. (5) can be rewritten as

\[
I_b = I_{b0} \cdot \exp \left( \frac{(V_A - V_D)}{nU_T} \right) + \Delta I_{b0} \cdot I_{b0} \cdot \exp \left( \frac{(V_A - V_D)}{nU_T} \right)
\]

If the leakage-current mismatch occurred in the exponential function generating cell Exp1 and Exp5 of the proposed cube – law circuit, based on eqn. (20) and according to eqns. (7 – 17), eqn. (18) can be rewritten as

\[
V_{av} \approx I_b \cdot \frac{2V_v}{(nU_T)^2} \cdot R + \left[ \frac{\Delta I_{b0}}{I_{b0}} \cdot \exp \left( \frac{2V_v}{nU_T} \right) - \frac{\Delta I_{b0}}{I_{b0}} \cdot \exp \left( -\frac{2V_v}{nU_T} \right) \right] \cdot R
\]

where \( I_{b0,1.5} \) are the leakage currents of the transistors in the exponential function generating cell Exp1 and Exp5, and \( \Delta I_{b0,1.5} \) are the mismatch currents between the leakage currents of the transistors in the exponential function generating cell Exp1 and Exp5, respectively. From eqn. (21), a non – linear deviation is generated. To avoid the deviation, careful layout consideration is necessary. Moreover, if the deviation in eqn. (21) is serious, since the leakage current \( I_{b0} \) is proportional to the aspect of the MOSFET, a long channel device can be used to improve it.

III. SIMULATION RESULTS

The proposed low-voltage and low-power CMOS cube – law circuit has been evaluated with the HSPICE simulation program, where a 0.35\( \mu \)m N-well CMOS 2P4M process was used in the simulation. The aspect ratios of the PMOS transistors in the proposed cube – law circuit are all \( \left( \frac{W}{L} \right) = \frac{5\mu m}{1\mu m} \). The threshold voltage for the PMOS transistor is about \(-0.7 \) V in our process and the supply voltage used in the simulation is 1.5 V. The simulations were performed with the bias voltage \( V_c = 0.82 \) V and in order to bias the PMOS transistors in the proposed circuit to operate in weak-inversion region, according to eqn. (6), the bias current \( I_b \) was set to 0.22 \( \mu A \). With the resistors \( R_1 \) and \( R_2 \) in eqn. (18) equal 100 k\( \Omega \), when the input voltage \( V_{in} \) varies from \( -100 \) mV to 100 mV, the corresponding frequency response is shown in Fig. 5. According to Fig. 4, the simulation results confirms the validity of eqn. (18).

![Fig. 4 DC transfer curve of the proposed cube-law circuit](image)

![Fig. 5 Frequency response of the proposed cube-law circuit](image)

To test the frequency response of the proposed cube – law circuit, the simulation was executed with the bias voltage \( V_c = 0.82 \) V, the DC component of the input signal is 0.1V, and the amplitude of the small signals was 0.01V, respectively. Also, a 10 pF capacitor was attached to the output of the proposed circuit as the load capacitance. The corresponding frequency response is shown in Fig. 5. From which, we observe that the 3- dB bandwidth of the proposed cube – law circuit is about 161 kHz. The major reason for the limited bandwidth of the proposed circuit is due to the weak-inversion operation of the MOSFETs. As
the frequencies of the input voltage are 1 k, 10 k, 50 k, and 100 kHz, respectively, the corresponding THD are shown in Fig. 6. The simulated maximum power consumption for the proposed cube – law circuit is 10.72 µW, which occurred at the bias voltage $V_{C} = 0.82$ V and the input voltage $V_{in} = \pm 100$ mV. The simulation results are consistent with the theoretical analysis given in eqns. (7 – 18). Finally, the performances of the proposed low – power and low – voltage cube – law circuit are summarized in Table II. References [4] and [10] are also included as comparisons.

![Fig. 6 THD for the proposed cube – law circuit](image)

**TABLE III**

<table>
<thead>
<tr>
<th>Work Item</th>
<th>Proposed</th>
<th>[4]</th>
<th>[10]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>MOSFET</td>
<td>JFET</td>
<td>BJT</td>
</tr>
<tr>
<td>Process</td>
<td>0.35µm CMOS 2P4M</td>
<td>NPDS402 (discrete device)</td>
<td>0.35µm BiCMOS</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.5 V</td>
<td>No needed</td>
<td>± 1 V</td>
</tr>
<tr>
<td>Low-voltage operation</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Input range</td>
<td>±100 mV</td>
<td>±0.6 V</td>
<td>0 – 1 V</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>10.72 µW</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Band width (@10 pF load)</td>
<td>161 kHz</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>THD</td>
<td>1.25% - 1.4% ($V_{in} = 5$ mV)</td>
<td>2.3 – 2.5% ($V_{in} = 7$ mV)</td>
<td>—</td>
</tr>
</tbody>
</table>

**IV. CONCLUSIONS**

In this paper, a new MOSFETs based low – power and low – voltage cube – law circuit has been presented. Simulation results have been given to confirm the validity of the theoretical analysis. The proposed cube – law circuit is expected to be useful in the design of frequency tripler, and other signal – processing circuits.

**REFERENCES**


